Code No: RT22054 **R13** SET - 1

II B. Tech II Semester Supplementary Examinations, Dec – 2015.
COMPUTER ORGANIZATION
(Com. to CSE,IT, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) What are the error detection codes? Convert the decimal 225.225 to octal and hexadecimal (4M)
   b) Explain the different timing diagrams associated with buses (4M)
   c) Explain the stack organization (3M)
   d) Explain the operation of Associative memory (4M)
   e) What is virtual memory (3M)
   f) Draw a flow chart that describes the CPU-I/O channel communication (4M)

PART –B

2. a) Draw the functional diagram of a computer and explain each block (8M)
   b) By using the required parity generator/checker circuit, explain how parity checking canbe used for the error detection (8M)

3. a) Explain the instruction cycle with help of a flow chart (8M)
   b) What is register transfer language? Explain the basic symbols used in register transfer (8M)

4. a) With a neat diagram, explain the instruction pipeline processing in RISC architecture (8M)
   b) Evaluate the arithmetic statement X = (A+B) * (C+D) using a general register computer with three address, and two address instruction format (8M)

5. a) Multiply each of the following pairs of signed 2's complement numbers using booth algorithm and bit pairing of the multiplier (Assume A is the Multiplicand and B is the Multiplier). (8M)
   A=010111 B=110110
   A=110011 B=101100
   b) Draw and explain the division of floating point numbers (8M)

6. a) Explain mapping in segmented page memory unit with the help of a block diagram. What do you understand by translation look aside buffer (8M)
   b) What is the difference between isolated IO and memory mapped I/O? State the advantages and disadvantages of each (8M)

7. a) Draw and explain the 8x8 omega switch network (8M)
   b) A DMA controller transfers 16-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at the rate of 2400 charaters per second. The CPU is fetching and executing instructions at an average rate of 1million instructions per second. By how much will the CPU be slowed down because of DMA transfer? (8M)

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